DC FAULT PROTECTION IN SHIPBOARD POWER SYSTEMS USING Z-SOURCE BREAKERS

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DC Fault Protection in Shipboard Power Systems using Z-Source Breakers

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Abstract
DC faults may cause severe disruptions in continuity of service to vital loads in a shipboard integrated power system, hence detection, isolation and protection against dc faults must be incorporated in both medium-voltage dc and low-voltage dc systems. A standard z-source breaker can identify and de-energize a faulty dc load on both buses quickly. However, until now, provisions for re-energizing have not been described. In this paper, a new z-source breaker is designed and control and detection techniques to identify the fault duration as well as to re-energize the load efficiently once the fault is cleared are developed. Dc fault characteristics on both medium- and low-voltage dc buses in a complete model of the all-electric-ship are demonstrated and the effective use of the new z-source breaker for the re-energizing process in protecting and restoring the continuity of ship service with a minimal effect is investigated.

Keywords: all-electric ship, fault detection, reconfiguration, MVDC.

I. INTRODUCTION

The US Navy anticipates an increase of integrated power systems (IPS) in the coming decades due to the projected propulsion and ship service power demands for future combatants. One of the architectures proposed [1] is the medium-voltage dc (MVDC) power generation system with zonal electrical distribution zones. To maintain continuity of service, protection against faults must be addressed quickly and efficiently in order to increase survivability. For a future shipboard MVDC architecture, traditional ac circuit breakers cannot be used to isolate a dc fault due to the difficulty in extinguishing dc arcs in the absence of a voltage or current zero-crossing [1-3]. The severity and location of the dc fault can be estimated from a load impedance, as proposed in [4], however this technique requires to inject a short current spike after the fault occurs.

A z-source breaker was introduced in [2,3] to quickly isolate a faulty load although it was not applied to IPS, and hence no fault detection strategies were proposed when the dc fault occurs on the MVDC bus. Fault isolation using the same breaker can also be applied to the low-voltage dc (LVDC) subsystem associated with the electrical distribution zones in an IPS. However, without some re-energizing procedure, the z-source breaker cannot be used for re-energizing a dc load after the fault is cleared because of the large current spike flowing through the thyristor, which could damage all other components.

The objectives of this work are to (1) investigate the effect of dc faults on the MVDC-bus and LVDC-bus loads propagating through the entire shipboard IPS; (2) establish dc fault isolation and load reconfiguration after the fault is cleared; and (3) develop effective z-source breakers and corresponding controllers for fault-isolation and reconfiguration purposes.
The paper is organized as follows. In section II, the modeling of a shipboard power system with a MVDC- and a LVDC-bus is briefly described. The modification of z-source breaker is also explained in detail in section II. In section IIIA the characteristics of dc faults on the two buses with emphasis on isolating the fault is investigated whereas in section IIIB the focus is on strategies to clear a fault. Section IV provides a brief summary.

II. MVDC AND LVDC POWER SYSTEM MODELING

The overall shipboard integrated power system (IPS) containing the MVDC and LVDC architectures is shown in Figure 1 as a one-line diagram.

![Fig.1. A one-line schematic diagram of shipboard Integrated Power System (IPS), that includes MVDC- and LVDC-buses; A and B denote locations of possible dc faults.](image)

The entire configuration consists of a half-plant power generation system (Gas turbine and Synchronous generator (SM)) and propulsion system (Induction machine (IM) and Torque controller) for the DDG-51 Arleigh Burke-Class, and one dc zone, connected by Power Conversion Module (PCM)-4 [6] for converting the voltage from 5kV to 1kV. All models are implemented in Matlab/Simulink; only the 3-phase passive rectifier and the active inverter from the prebuilt “SimPower Systems” toolbox are used in the generation and propulsion units. A discrete time solver with a fixed time step of 5 μs is applied to all simulations to handle the fast switching of the inverter and PCM-4.

A. MVDC Modeling

The power generation unit supplies the MVDC voltage of 5kV connected to the propulsion and PCM units. A simplified Gas Turbine (GT) directly coupled with a 3-phase, 60-Hz Synchronous Machine (SM) through the same shaft provides a maximum power of 21MW. GT’s speed and MVDC are maintained at their nominal values by a speed governor and exciter with a linear droop, respectively. For the propulsion unit, a 3-phase 15-Hz, 19MW Induction Machine (IM) controlled by the torque trim controller is directly coupled with a fix-pitch propeller, experiencing hydrodynamics force. The detailed model can be found in the literature [5]. The dynamic models can capture both fast transient and slowly-varying steady-state responses during critical load conditions, such as an ac or a dc fault.

B. LVDC Modeling

The medium-voltage dc of 5kV is efficiently converted to the low-voltage dc of 1kV using the PCM-4. It consists of (1) a double-ended forward isolated converter, which could reduce the switch rating, component voltage rating, and switching stress, and (2) a power control module, which helps coordinating the power among PCM-4 modules and maintaining output voltage of 1kV at the same time. In this paper, the switching frequency of the forward converter is fixed at 2 kHz; it has been shown that PCM-4 operates with a power loss less
than 20 percent of its nominal power consumption for various switching frequencies. More details on the PCM-4 can be found in [6].

C. Z-Source Breaker Modeling

A unique topology of impedance-source or z-source converter was originally proposed in [7,8] to overcome the disadvantages of traditional voltage- and current-source converters in terms of efficiency and ripple noise reduction. Also, the z-source converter can be operated either as buck or boost inverter that covers a wide range of input voltage, including zero voltage, by controlling the duty cycle of the PWM inverter. The unique characteristics of the z-source converter, allowing a shoot-through state or short-circuit of dc bus, is the main advantage for using it in handling dc faults.

Circuit diagrams of the classic z-source and new z-source breakers, separated from an R-C load by a short-circuit fault, are provided in [2,3]; we have modified the new z-source breaker as shown in Fig. 2. The z-source breaker is composed of a thyristor (SCR), diodes and resistor, and a crossed L-C connection. In the original z-source breaker, the crossed L-C circuit lies across both the forward and return paths of the dc source. In the new z-source breaker, the crossed L-C circuit is placed only in the dc-source forward path such that the return path or common ground can be established for all dc sources and loads. A disadvantage of the z-source breakers described in [2, 3] is that they cannot be used for re-energizing the load after the fault is cleared. There will be a large current spike through the SCR, when the dc source reconnects with the breaker. To eliminate the SCR current spike, we modified the z-source breaker by adding a resistor in series with the crossed capacitors, as shown in Fig. 2. This modification is similar to a soft-starting method in a feedback control of an up/down converter [9] to limit the rising rate of the duty ratio and to reduce stresses during the start-up period.

![Fig. 2. Modified topology of the new z-source breaker in [3] by adding a resistor in series with the crossed capacitor.](image)

Table 1. Turn-off performance comparison: System parameters for z-source breaker.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
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</thead>
<tbody>
<tr>
<td>$V_s$ = 6kV</td>
<td>L = 200 $\mu$H</td>
</tr>
<tr>
<td>$R_{\text{load}}$ = 6 $\Omega$</td>
<td>C = 125 $\mu$F</td>
</tr>
<tr>
<td>$R_{\text{fault}}$ = 1 m$\Omega$</td>
<td>$C_{\text{load}}$ = 1 mF</td>
</tr>
<tr>
<td>$\Delta t_{\text{fault}}$ = 0.1 s</td>
<td>$R_d$ = 0.1 $\Omega$</td>
</tr>
<tr>
<td>$R_c$ = 0.5 $\Omega$</td>
<td></td>
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</table>

The principles of operation of the z-source breaker can be explained through simulation of dc short-circuit or fault occurring on the R-C load. Table 1 provides the system parameters of this simulation. We assume that the dc short circuit happens between 0.05 and 0.06 second and the thyristor (SCR) is manually turned off 0.1 ms after the fault occurs. We have simulated the performance of both z-source breakers presented in [3] as well as the modified new z-source breaker as shown in Fig. 2. Without our modification, when the fault suddenly
occurs, the fault current will rush through the two cross capacitors in a few microseconds, causing an immediate increase in $i_C$ to match the magnitude of $i_L$ and a sudden drop of $i_{SCR}$ to zero. This, in turn, will cause the SCR to commutate off and the $V_{SCR}$ to increase suddenly to match the source voltage; then, the output voltage will drop to zero. However, $i_L$ and $V_C$ cannot be changed spontaneously, so they gradually increase and decrease, respectively. During this commutation-off period of about 0.1 ms, we disconnect the SCR gate current in order to switch off the SCR or to isolate the dc fault. Otherwise, the SCR will conduct a large fault current after $V_{SCR}$ becomes negative, which may lead to damages in the breaker as well as in the downstream loads.

In the original z-source breaker, both $i_L$ and $i_C$ supply the fault current and block the current from the voltage source during the commutate-off period; then, the two series L-C circuits in parallel will start resonate in the short-circuit loop after switching off the SCR. The remaining energy will be dissipated in the two diode and inductance loops. In the new z-source breaker, during the commutate-off period, both $i_L$ and $i_C$ as well as the current from the dc source through two series L-C circuits supply the fault current. When the SCR turns off, two series L-C circuits in parallel on the forward path will start resonate and block the current from source at the same time until all energy is dissipated in two diode and inductance loops. Another major difference between the original and the new z-source breakers is that the new z-source breaker draws a large source current ($i_S$) during the commutate-off period, but the original z-source breaker does not.

With the previous z-source breaker topologies without a series R-C branch, $i_C$ jumps suddenly to maintain continuous $V_C$ when the connection with the dc source is re-established at 0.06 second right after the fault is cleared. As a result, there exists a 3MA spike in $i_{SCR}$ as well, which could damage SCR (plots not shown here); although in practice this spike would be limited by the capacitor's equivalent series resistance (ESR). To significantly reduce the $i_{SCR}$ spike during the re-energized period, 0.5Ω resistors are added in series with $C$, so the resistor helps limiting the current flowing through $C$. As shown in Fig. 3, the $i_{SCR}$ peak reduces to about 12kA, which is limited by the gradually increasing inline inductor current, $i_L$, during this re-energizing period. The simulation results demonstrate that the modified z-source breakers could be employed for both de-energizing and re-energizing processes to isolate the dc fault and to re-establish the source with the dc load again.

![Fig. 3. Waveform of the modified new z-source breaker for de-energizing and re-energizing operations.](image-url)
Fig. 3 shows that the SCR peak voltage and current of the modified z-source breaker are less than the actual SCR specification in Table 2. Moreover, $i_{\text{SCR}}$ increases to 11 kA within 1 ms interval, hence, the rate of rise of on-state current is about 11 A/$\mu$s, which is smaller than the SCR specification. Thus, the thyristor can operate safely without damage.

<table>
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<tr>
<th>Specification of semitronics power thyristor – TN880CH series [10].</th>
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<tbody>
<tr>
<td>Repetitive and Non repetitive peak reverse voltage</td>
</tr>
<tr>
<td>RMS value of on-state current</td>
</tr>
<tr>
<td>Peak one cycle surge (non repetitive) current</td>
</tr>
<tr>
<td>Critical rate of rise of on-state current</td>
</tr>
<tr>
<td>Critical rate of voltage rise</td>
</tr>
<tr>
<td>Holding current</td>
</tr>
<tr>
<td>Turn-off time</td>
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### III. DC FAULT ISOLATION AND PROTECTION

With the modified new z-source breakers on both MVDC and LVDC buses, a faulty load can be automatically identified and isolated from the other components within the **first millisecond** of the dc fault to avoid propagation of the fault effect. After the fault is cleared, the modified new z-source breaker can then automatically reconnect that load to the bus again to resume its normal operation.

#### A. DC Fault Isolation

A simple criterion for the dc fault isolation is to turn off the z-source breaker by detecting a sudden increase of the voltage across the SCR ($V_{\text{SCR}}$) during the commutated turn off period, when $i_{\text{SCR}}$ goes below its holding current of 200 mA within a turn-off time of 0.25 ms [3]. When $V_{\text{SCR}}$ rises above the threshold voltage of 500 V, taking longer than 0.25 ms, then the thyristor gate current can be removed. Therefore, the faulty dc load can be detached from the upstream components for isolation.

Here we investigate the effect of a relatively long duration dc-fault ($\Delta t_{\text{fault}} = 0.1$ second), which we first analyzed systematically without any isolation (results not shown here for brevity). All components operate in their steady-state condition and then the non-ground shorted-circuit or dc fault suddenly occurs on the PCM-4 connecting to the MVDC bus, shown by the blue cross at location A in Fig. 1, at 25 seconds. When the z-source breaker on the MVDC bus detects an instantaneous jump of the $V_{\text{SCR}}$, as shown in Fig. 6, it automatically removes the thyristor gate current within 0.25 ms following the fault event. The fault isolation using the breaker can substantially reduce the jump in the SM torque and angular speed by more than 15 times (from 150 kN-m without turning off the breaker to less than 10 kN-m with the breaker turned off) and 20 times (from 12 rad/s without turning off the breaker to 0.6 rad/s with the breaker turned off), respectively. In addition, there is no disturbance on the induction motor IM. Besides that after the z-source breaker isolates the PCM-4 from the MVDC bus, less power is drawn from the SM, which leads to a smaller SM torque as shown in Fig. 4. This result shows that the power generation unit can survive the dc fault with the breaker isolation. According to Fig. 5, the MVDC voltage ($V_{\text{MVDC}}$) decreases less than 20 percent of its nominal value and the quick fault isolation prevents $V_{\text{MVDC}}$ to drop to zero, compared to the case without fault isolation. The $i_{\text{MVDC}}$ spike of 5 kA, in Fig. 5, is half of the $i_{\text{MVDC}}$ spike of 10kA without fault isolation, within the first few milliseconds of the fault. Since the PCM-4 is disconnected from the MVDC bus after the dc fault, the LVDC voltage and current ($V_{\text{LVDC}}$ and $i_{\text{LVDC}}$) in Fig. 5 as well as the SCR current ($i_{\text{SCR}}$) of the breaker on the LVDC bus gradually drop to zero in less than 20 ms. There is no any significant effect on the ac voltage and current of either the SM or IM. After the breaker on
the MVDC bus is turned off, its SCR must carry the reverse MVDC voltage of 5 kV dropping across it to block the current flowing through, as shown in Fig. 6.

![Graph of SM T and SM ω](image-url)

**Fig. 4** DC Fault Isolation on MVDC bus: Torque (T_e) and speed (ω_r) of SM and IM when the MVDC bus is subjected to the DC fault (Δt_Fault) of 0.1 second.

![Graphs of DC voltage and current](image-url)

**Fig. 5** DC Fault Isolation on MVDC bus: DC voltage and current of MVDC- and LVDC-buses when the MVDC bus is subjected to the dc fault (Δt_Fault) of 0.1 second.

![Graphs of modified z-source breaker](image-url)

**Fig. 6** DC Fault Isolation on MVDC bus: Waveform of the modified new z-source breaker on the MVDC bus when the MVDC bus is subjected to the dc fault (Δt_Fault) of 0.1 second.

For the dc fault occurring on the resistive load connecting to the LVDC bus, the z-source breaker can also limit the fault propagation to other upstream components. The dc-fault location is represented by the red cross at location B, as shown in Fig. 1. Similarly, when the voltage across the SCR, used as a fault detection signal, increases above 500 V, the thyristor gate current is removed. With a de-energizing of the faulty load, the disturbance on both SM torque and speed are much smaller than those of the MVDC fault isolation due to a farther location of the fault from the power generation and propulsion units. According to Fig. 7, a voltage drop of 400 V and a current spike of 600 A happen only on the LVDC bus, while the voltage and current of the MVDC bus (V_{MVDC} and i_{MVDC}) are only slightly disturbed. Also,
we notice that when one of the parallel resistive loads is disconnected from the LVDC bus, the oscillation of the MVDC current ($i_{MVDC}$) in Fig. 7 and the SCR current ($i_{SCR}$) of the breaker on the MVDC bus decrease by half because only half power is drawn from the MVDC bus. After the breaker on the LVDC bus is switched off, its SCR must carry a reverse LVDC voltage of 1 kV across it to block the current passing through the faulty load, as shown in Fig. 8. We also observed that the SCR voltage of the z-source breaker on the MVDC bus is disturbed slightly during this fault isolation.

Fig. 7 DC Fault Isolation on LVDC bus: DC voltage and current of MVDC- and LVDC-buses when the LVDC bus is subjected to the dc fault ($\Delta t_{\text{Fault}}$) of 0.1 second.

Fig. 8 DC Fault Isolation on LVDC bus: Waveform of the modified new z-source breaker on the LVDC bus when the LVDC bus is subjected to the dc fault ($\Delta t_{\text{Fault}}$) of 0.1 second.

B. DC Fault Protection

The fault duration can be determined by monitoring the dynamics-response variation of the SCR voltage ($V_{SCR}$) of the z-source breaker during the dc fault. The variance of $V_{SCR}$ should not be computed instantaneously, but it must be calculated over a certain time frame at a lower sampling rate as well. Implementation of the $V_{SCR}$ variance computation using a buffer size of 128 in Matlab/Simulink is shown in Fig. 9. Circuit memory is needed to realize the variance computation in the actual circuit. Nevertheless, the $V_{SCR}$ variance varies over a wide range during the fault period before dropping to zero after the fault is cleared, as seen in Fig. 10 for four different fault durations. Therefore, two-level Gaussian filters are needed to eliminate a high-frequency fluctuation in the $V_{SCR}$ variance so that a decreasing signature of the $V_{SCR}$ variance to zero can be notably revealed, as shown in Fig. 11, for four fault durations. The Matlab/Simulink implementation of the SCR gate control using the $V_{SCR}$ variance as the fault detection indicator is shown in Fig. 12. In the following study, the fault
duration detection for the load re-energizing process is tested for four different dc fault durations of 0.005, 0.01, 0.05, and 0.1 seconds.

Fig. 9 Implementation of $V_{\text{SCR}}$ variance computation in Matlab/Simulink using the buffer, variance, and unbuffer blocks.

![Fig. 9](image)

Fig. 10 The variance of the voltage dropped across the SCR ($V_{\text{SCR}}$) varies over a wide range during the dc fault duration of 0.005, 0.01, 0.05, and 0.1 seconds.

![Fig. 10](image)

Fig. 11 After passing through the Guassian filters, the filtered variance of the voltage dropped across the SCR ($V_{\text{SCR}}$) varies smoothly during the dc fault duration of 0.005, 0.01, 0.05, and 0.1 seconds.

![Fig. 11](image)

Fig. 12 Implementation of the thyristor gate control of the z-source breaker to de-energize and re-energize the dc load in Matlab/Simulink.

![Fig. 12](image)

In the case of dc fault occurring on the load connecting to the MVDC bus, the thyristor gate control of the z-source breaker can automatically de-energize and re-energize the faulty load to protect the power generation. This gate control can detect a fault instance to switch off the breaker within 0.25 ms and identify an instance of the fault clearance to turn the breaker back on. Compared to results of Fig. 4, the SM angular speed is less disturbed when the faulty connection on the MVDC bus is shortly re-established shortly after clearing the fault, which leads to a small interruption of SM torque. There are small spikes of 2 kA in $i_{\text{MVDC}}$ and a small drop of 500 V in $V_{\text{MVDC}}$ during the re-energizing process for any fault duration. The voltage and current of the LVDC bus can recover from the dc fault, as shown in Fig. 13. This is the main advantage of the dc fault protection using the z-source breaker that both MVDC and LVDC buses can survive the fault without any damage and operate normally again once the fault is cleared. However, there is a SCR current spike of 5 kA in Fig. 14 when the modified new z-source breaker on the MVDC bus instantaneously re-connects the PCM-4 with the MVDC bus, which is caused by the shoot-through state of the breaker. The z-source breaker on the LVDC bus losses power during this dc fault period when $i_{\text{SCR}}$ equals to zero.
Fig. 13 DC Fault Protection on MVDC bus: DC voltage and current of MVDC- and LVDC-buses subjected to 4 different dc-fault durations ($\Delta t_{\text{Fault}} = 0.005, 0.01, 0.05, \text{and } 0.1 \text{ second}$).

Fig. 14 DC Fault Protection on MVDC bus: Waveform of the modified new z-source breaker on the MVDC bus subjected to 4 different dc-fault durations ($\Delta t_{\text{Fault}} = 0.005, 0.01, 0.05, \text{and } 0.1 \text{ second}$).

Using the modified new z-source breaker to protect against the dc fault, one of the parallel resistive loads supplied by the LVDC bus can be disconnected during the fault and reconnected once again after the fault. Therefore, the entire power system can survive the dc fault on the LVDC bus with a minimum disruption. Our simulations show that in this case the SM torque drops slightly during the breaker turn-off period because of less power consumption. Re-energizing the faulty load can significantly reduce the perturbation on the SM angular speed. We also note that we did not observe any perturbations on IM torque or speed.

The MVDC- and LVDC-bus voltage and current have the same characteristics during the fault isolation as previously shown in Fig. 7. Once the faulty resistive load is re-energized, $V_{\text{LVDC}}$ drops by 10% of its nominal value, while $V_{\text{MVDC}}$ jumps slightly and approaches the same oscillation magnitude before the fault and vice versa for the MVDC current. During the fault, the SCR current of the breaker on the LVDC bus drops to zero and the SCR must carry the reverse LVDC voltage of 1 kV to block the power flowing through the faulty load. According to Fig. 15, there is a current spike of 1 kA in the SCR when the z-source breaker reconnects the resistance load with the LVDC bus again after the fault is cleared. The current flowing through the SCR on the MVDC bus is half during the fault de-energizing process since the power drawn from the MVDC bus is also reduced by half.
IV. CONCLUSION

Faults in dc shipboard power systems have only recently been analyzed for the MVDC system [11] but no specific strategies in detecting, isolating or clearing the fault have been formulated. In the present work, all three important steps have been addressed and an existing z-source breaker for implementing them has been modified. In particular, performance of four different z-source designs including the two designs first proposed in the literature are compared and it was concluded that the design introduced herein is the most suitable for the shipboard IPS. Subsequently, an end-to-end model of MVDC IPS with the addition of a low-voltage dc (LVDC) subsystem was employed and faults in the MVDC bus and in the LVDC bus were considered independently. It was first demonstrated that faults of different durations in less than 0.25 ms could be detected and isolated by monitoring the voltage across the thyristor in the z-source breaker. Subsequently, a technique was presented to estimate the duration of the fault automatically and hence clearing the fault and re-energizing the loads affected by the fault. To this end, the variance of the voltage in the thyristor computed over a certain time history was used; this procedure was implemented using buffer/unbuffer to resample the $V_{SCR}$ in Matlab/Simulink. It was found that re-energizing the faulty loads using this technique reduces significantly the perturbations on the synchronous generator and the induction machine while the voltage at the MVDC and LVDC buses change by less than 10% of their nominal values.

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