Abstract - The medium-voltage dc (MVDC) architecture shows potential for future ship power systems. Components of the MVDC system are fairly well established; with the exception of circuit breakers. The main problem with the breakers in dc systems is the absence of a zero crossing in the current needed to extinguish an interrupting arc. Options for breakers in MVDC systems include over-sizing traditional ac breakers, hybrid mechanical/semiconductor breakers, and solid-state breakers. The recently introduced z-source breaker is most similar to the solid-state breaker, but has the additional feature of automatically responding to faults quickly and without the need for fault detection. Furthermore, the z-source breaker isolates the generation source from the fault current. This paper presents detailed analysis of the z-source breaker as well as variations on the topological structure. The various breaker options are validated through detailed simulation.

I. INTRODUCTION

This paper explores the recently invented z-source dc circuit breaker [1] which utilizes a principle defined by the introduction of the z-source inverter [2]. A number of researchers have studied the z-source inverter and documented results in recent publications pertaining to comparison with existing topologies [3], operating mode analysis [4], and variations on the topology [5]. By using a crossed L-C circuit arrangement, the z-source inverter introduced an additional shoot-through state where all inverter transistors could be gated on. The z-source breaker operates in the shoot-through state during a fault; thereby avoiding excessive upstream currents. Furthermore, the z-source breaker can automatically respond to faults, providing fast isolation without fault detection [1]. Forced commutation of the z-source breaker, where a load can be switched off, is also possible so as to allow coordination with other breaker systems. The advantages of this new breaker make it an ideal candidate for future naval ship power systems which employ the medium-voltage dc (MVDC) architecture [6].

This paper first presents an overview of the traditional z-source breaker. One of the characteristics of the z-source circuit is that one of the inductors in the crossed connection ends up in the return path of the dc source. This can be seen as a disadvantage in systems where a common ground is preferred. To address this, a completely new topology of the z-source breaker is presented herein. Analysis of this new breaker is presented along with simulation examples.

II. THE CLASSIC Z-SOURCE DC CIRCUIT BREAKER

Figure 1 shows the schematic diagram of the traditional z-source MVDC circuit breaker [1] which consists of an SCR, a crossed L-C connection, diodes, and resistors as indicated in the dashed box. The system load is represented by the R-C circuit consisting of $R_c$ and $C_f$. A fault is depicted by the conductance $G_f$. The z-source L-C connection was initially suggested as a novel type of inverter input circuit [2] that can cause the inverter to operate in boost, as well as the standard buck, mode. The reason for this is that the z-source allows another state wherein the inverter can short-circuit its dc bus. Herein, this feature is adopted for fault handling in MVDC power systems. When the fault occurs in this system, there is no direct short of the capacitor voltages, because of the inductors in the z-source circuit. The breaker components act together to quickly mitigate faults in a dc system. When a fault occurs at the output of a z-source breaker, current sources into the fault from the downstream system capacitance $C_f$ as well as from the z-source capacitances as shown by the fault conduction path in Figure 2.
The full set of z-source waveforms during a fault are shown in Figure 3. Therein, the variables are as defined in Figure 1. The parameters and operating conditions for this example are given in Table I with \( R_p \) being the resistance in series with the diodes. The system is operating in the steady-state and the fault conductance is ramped from zero to \( 1/2f_0R \) in a time interval of \( \Delta t \). A portion of the fault current will come from the z-source breaker capacitances. Initially, in the transient state, the inductor keeps the current \( i_L \) constant as seen in Figure 3. The conduction path is then through the z-source capacitors and back to the source as shown in Figure 2. Therefore, the capacitor current \( i_C \) is seen in Figure 3 to increase until it matches \( i_L \). At this point, \( i_{SCR} \) will go to zero causing the SCR to commutate off. In this way, the z-source breaker creates the zero crossing, typically absent in dc power systems; but needed to properly isolate the fault current. A simple circuit can then detect that a SCR has switched off and remove the gate current from the SCR. After the SCR switches off, the z-source components are configured as two series L-C branches connected to the load and fault. These circuits start a resonance where they are supplying the fault, but since the source has been disconnected and the fault impedance is low, the output voltage collapses to zero. By KVL, with the output voltage at zero, \( v_C \) must be equal to \( v_L \). In Figure 3, it can be seen that the inductor and capacitor voltages become equal when the output voltage goes to zero. Also, by KVL, it can be shown that when these voltages reach half of the source voltage \( v_s \), the SCR will become forward biased. Therefore, the time when \( v_{SCR} \) is positive is the amount of time available for the control circuit to remove the gate pulse and the SCR to undergo its reverse recovery transient. The resonance continues until the inductor voltages attempt to go negative. At this point, the diodes will turn on. The current in the capacitor will go to zero and the current will continue in the inductor/diode/resistor loop until it decays to zero. It can also be shown by KVL that since the inductor voltage does not go negative, the SCR voltage will not go above the source voltage. Figure 3 also shows the source current \( i_{SCR} \) going to zero when the fault occurs, as desired. After the SCR goes off, the fault has successfully been isolated.

| TABLE I. SYSTEM PARAMETERS. |  
|-----------------------------|--|---|---|
| \( v_s \) = 6 kV | \( R_p \) = 20 m\( \Omega \) | \( \Delta t \) = 0.1 ms |
| \( L = 200 \mu H \) | \( C = 125 \mu H \) | \( R_f = 0.1 \Omega \) |
| \( R_f = 6 \Omega \) | \( C_f = 1 mF \) |
A. Fault Interval

The fault interval is defined as the time in which the SCR current goes to zero immediately after a fault. This is depicted as interval A in Figure 6. Neglecting the SCR voltage drop and the inductor resistance, the steady-state SCR current is

$$I_{SCR} = \frac{v_i}{R_i} \quad (1)$$

At this stage of the analysis, the source inductance will also be neglected. The initial transient is based on the fault conductance. For the purpose of this analysis, the conductance is assumed to ramp from zero to a final value with a ramp rate of

$$K = \frac{1}{\Delta t \cdot R_{\rho}} \quad (2)$$

where $\Delta t$ is the time for the conductance to ramp to its final value which is the reciprocal of $\Delta t$. For the first part of the analysis, it is assumed that the inductor current remains constant. Then, the transient fault current takes a path supplied by the capacitances as displayed in Figure 5. Since the fault current is related to the output voltage by

$$i_f = G_f \cdot v_o = K v_o t \quad (3)$$

The portion of fault current supplied by the breaker capacitance and the load capacitance can be determined using the current division rule. Then, the change in output voltage can be found using linearization of the load capacitance equation. From there, the currents in the system can be computed [1] resulting in

$$i_L = v_s K t - \frac{v_s C K^2}{2C_i} t^3 \quad (4)$$

$$i_c = v_s C S K t - \frac{v_s C K^2}{2C_i} t^3 \quad (5)$$

$$i_L = I_{SCR} + v_s C K \frac{t^5}{12LC_i} \quad (6)$$

$$i_{SCR} = I_{SCR} - v_s C S K t + \frac{v_s C K}{12LC_i} (6LC_s K + 1) t^3 \quad (7)$$

where

$$C_s = \frac{C}{C + 2C_i} \quad (8)$$

$$C_d = \frac{2C_i}{C + 2C_i} \quad (9)$$

Using (7), the exact commutation point can be computed in response to a specific fault. For example, using the parameters and operating conditions of Table I, the time at which commutation occurs can be calculated as 7.08 $\mu$s and is found to be 7.03 $\mu$s from detailed simulation. Equation (7) can also be used to determine the conditions under which commutation will occur and the amount of z-source capacitance required for commutation [1].

B. Z-Source Breaker Resonance Interval

Once the SCR has commutated off, the z-source circuit appears as shown in Figure 7. At this stage, a resonance occurs between the z-source inductors and capacitors. This is seen in Figure 6 and labeled as interval B. At the beginning of this interval, each L-C branch has an initial current determined by (1). The inductor and capacitor voltages in this interval illustrate the resonance. As seen, the inductor voltage resonates to a peak and then to zero while the capacitor voltage rises from zero to a peak value. The resonance is distorted by the fact that the output voltage collapses at the beginning of this interval. When the inductor voltage starts to go negative, the diodes conduct the inductor current. Since the resistance in series with the diode is relatively small, the inductor voltage is practically held at zero.
C. Source Resonance Interval

In the final interval, defined as interval C in Figure 6, the inductor voltages are clamped at zero, the output voltage has collapsed, and the capacitors have charged to a value equal to the source voltage. At this point, the source inductance has a significant effect on the circuit operation. Figure 8 shows the equivalent circuit for this mode of operation where the source inductance is denoted by $L_s$.

With the example shown in Figure 6, the source inductance was negligible and therefore, the voltages are relatively flat in this interval. However, if the source inductance is increased, a resonance will occur in interval C. Figures 9 and 10 show the z-source breaker waveforms for cases where the source inductance is $L_s = 10 \mu H$ and $L_s = 50 \mu H$ respectively. As can be seen, an increase in source inductance leads to an increase in capacitor voltage oscillations. This is significant in that the SCR voltage will reach a higher peak value and this must be taken into account when selecting semiconductor devices. For systems with a high amount of source inductance, an L-C filter with damping [7] can be placed at the input to the z-source breaker to counteract this effect.
IV. CONCLUSION

In this paper, the recently published work on the z-source dc circuit breaker is first reviewed. This breaker utilizes the z-source L-C circuit connection along with a main path SCR to automatically respond to faults. Compared to traditional solid-state breakers, it has a faster response to faults and does not allow the fault current to be reflected back to the source. Next, a new topology of the z-source breaker has been introduced. This new topology does not place an inductor in the return ground path. Therefore, power systems that utilize this breaker can have common ground throughout. The fault operation intervals of the new z-source breaker are analyzed and demonstrated through computer simulation.

REFERENCES